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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,803	SYED ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,30,32-36,39 and 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,30,32-36,39 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 4, 2004 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 4-6, 30, 32-36, 39 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 6, 30, 34, 36 and 41, the phrase "any" renders the claim indefinite because it contains one, some, or all indiscriminately number or amount and unlimited or unmeasured quantity.

Regarding claims 4-5, 32-33, 35, and 39 are also rejected because of depending on claims 1, 6, 30, 34, and 36 respectively, containing the same deficiency.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 4-5, 30, 32-33 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al. (US PAT. 6,754,781 herein after Chauvel) in view of Tran (US PAT. 5,900,012).

Regarding claim 1, Chauvel disclosures a cache memory system, i.e., configurable cache (500, figure 4), comprising a plurality of memory locations for storing data, i.e., tag (502, figure 4), and addresses, i.e., data array (506, figure 4), associated with the data, wherein the memory locations are organized as two or more ways, i.e., four-way associative cache (col. 6 lines 40-62), and at least one controller, i.e., cache controller (530, figure 4), that enables a first device, i.e., processor core, to access a first way selected from the two or more ways (col. 8 lines 31-44), and enables a second device, i.e., direct memory access circuit to access a second way selected from

two or more ways (col. 17 line 27 through col. 18 line 8), wherein the first and second ways can be accessed concurrently by the first and second devices, respectively (col. 18 line 9 through col. 19 line 39). Although Chauvel does not clearly discloses the configurable cache system is capable to allow the first device can access any location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access any location in the second way and the first device is blocked from accessing the second way during access by the second device, Chauvel teaches the configurable cache comprising valid bit (504) in each of the cache index wherein the valid bit is indicated the corresponding cache line is valid/invalid, and further communicate with the hit/miss logic (510) to respond to the requested device, thus, Chauvel also teaches, the direct memory access circuit is only operated when the cache line is invalided, and further local the corresponding valid address in the lower level memory (col. 20 line 6 through col. 22 line 6). In addition, as the example disclosures in Tran, a storage device, i.e., cache memory system as define in figure 2 comprising a direct-mapped cache and a set-associative cache which it's corresponding tag array and data array, respectively, wherein both direct-mapped cache and set-associative are accessed in parallel to response to the request from the request unit (40, figure 2), by it's corresponding tag array and data array and controller, respectively (col. 6 lines 5-25 and col. 8 line 51 through col. 9 line 40). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the configurable cache system of Chauvel is capable to allow the first device can access any location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can

access any location in the second way and the first device is blocked from accessing the second way during access by the second device, because it provides higher hit rates and low access time.

Regarding claims 4-5, Chauvel disclosures the combination with the first and second devices, wherein the first device includes a processor, i.e., processor core, configured and arranged to access the memory locations (col. 8 lines 31-44), and wherein the second device includes a data transfer engine comprising a DMA controller, i.e., direct memory access circuit, configured and arranged to transfer data between the memory locations and a lower-level memory (col. 15 line 35-col. 16 line 6 and col. 18 line 9 through col. 19 line 19).

Regarding claim 30, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 32-33, the limitation of the claims are rejected as the same reasons set forth in claims 4-5.

Regarding claim 41, the limitation of the claim are rejected as the same reasons set forth in claim 1.

6. Claims 6, 34-36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al. (US PAT. 6,754,781 herein after Chauvel) in view of Donoghue et al. (US PAT. 6,751,700 hereinafter Donoghue).

Regarding claim 6, Chauvel disclosures a cache memory system, i.e., configurable cache (500, figure 4), comprising a plurality of memory locations for storing data, i.e., tag (502, figure 4), and addresses, i.e., data array (506, figure 4), associated with the data, wherein the memory locations are organized as two or more ways, i.e., four-way associative cache (col. 6 lines 40-62),

a plurality of cache outputs for providing data retrieved from the memory locations (figure 4), a first device, i.e., processor core, to access a first way selected from the two or more ways (col. 8 lines 31-44), and enables a second device, i.e., direct memory access circuit to access a second way selected from two or more ways (col. 17 line 27 through col. 18 line 8), wherein the first and second ways can be accessed concurrently by the first and second devices, respectively (col. 18 line 9 through col. 19 line 39). Although Chauvel does not clearly disclosures both the first and second are multiplexer, and the first and second multiplexers having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs coupled to the plurality of cache outputs, Chauvel disclosures the direct memory access circuit comprising multiplexer (1612) controlled by mode signal to select dest/src register for providing addresses to external memory when DMA mode, thus, it is well know in the art that processor is comprising a multiplexer as one of the elements to perform input/output operations between the processor and another device. In addition, as an example in the set-association cache of Donoghue, a plurality of Mux connected to each of the data array and outputting the data to the line (37), (figure 3 and col. 4 line 12-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the cache memory of Chauvel in having the first and second are multiplexer, and the first and second multiplexers having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs coupled to the plurality of cache outputs, as disclosures above, because it implement the cache memory with higher hit ratio and low access time.

Regarding claim 34, the limitation of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 35, Chauvel disclosures the cache memory system further comprising step of controlling first and second multiplexers to concurrently select as their respective outputs data from different ones of first and second ways of the cache (col. 17 line 26 through col. 18 line 15).

Regarding claim 36, the limitation of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 39, the limitation of the claim are rejected as the same reasons set forth in claim 35.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Palanca et al. (US PAT. 6,772,291) disclosures method and apparatus for cache replacement for a multiple variable way associative cache (abstract).

Sakai (US PAT. 6,131,143) disclosures multiple way associative storage type cache memory (abstract).

Pickett (US PAT. 5,893,146) disclosures cache structure having a reduced tag comparison to enable data transfer from the cache (abstract).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2186

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